INTEGRATED CIRCUIT MEMORY SYSTEMS HAVING PROGRAMMABLE SIGNAL BUFFERS FOR ADJUSTING SIGNAL TRANSMISSION DELAYS AND METHODS OF OPERATING SAME

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of Korean Application No. 2000-50164, filed August 28, 2000, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates generally to the field of integrated circuit devices, and, more particularly, to signal distribution circuitry used in integrated circuit devices.

Signal transmission times between respective memory devices in a memory system may differ based on the positions of the memory devices. The signal transmission times between signals following similar length paths may also differ due to skew between the signals. Differences in signal transmission times and/or skew may reduce a valid data window for determining a maximum operating frequency and may increase setup times and hold times for signals.

To compensate for skew, conventional memory devices and controllers may include a phase locked loop (PLL) or a delay locked loop (DLL). Unfortunately, this may increase the size of the memory device. Also, designing the PLL or DLL may cause difficulties in developing the memory device.

FIG. 1 is a schematic of a conventional memory system that illustrates different signal delays between modules and/or memory devices. **FIG. 2** is a timing diagram that illustrates skew between signals and the reduction of a valid data window due to the skew.

Referring now to **FIG. 1**, a conventional memory system comprises a plurality of memory modules **11**, **13**, and **15** controlled by a memory controller **10**. The transmission time of a signal between a memory module **11**, **13**, or **15** and the memory controller **10** varies according to the position of the memory module **11**, **13**, or **15**. For example, the transmission time of a signal between the memory module **11** and the memory controller **10** is **t0** and the transmission time between the memory module **15** and the memory controller **10** is **t10**.

Memory module **11** comprises a plurality of memory devices **21**, **23**, **25**, and **27**. The transmission time of a signal between the memory controller **10** and one of the memory devices **21**, **23**, **25**, or **27** varies according to the position of the memory device **21**, **23**, **25**, or **27**. For example, the transmission time of a signal between the memory device **21** and the memory controller **10** is **t1** and the transmission time between the memory device **27** and the memory controller **10** is **t4**.

Thus, the transmission time of a signal between the memory controller **10** and a memory module **11**, **13**, or **15** varies according to the position of the memory module. Furthermore, the transmission time of a signal between the memory controller and a memory device **21**, **23**, **25**, or **27** varies according to the position of the memory device. Similar principles apply to memory module **13**, which comprises memory devices **31**, **33**, **35**, and **37**, and memory module **15**, which comprises memory devices **51**, **53**, **55**, and **57**.

Referring now to **FIG. 2**, time **t1** illustrates a data setup time that is increased due to skew between signals and/or differences in signal transmission time between the memory controller **10** and the memory modules **11**, **13**, and **15** and/or the memory devices contained therein. Time **t3** illustrates a data hold time that is increased due to skew between signals and/or differences in signal transmission time between the memory controller **10** and the memory modules **11**, **13**, and **15** and/or the memory devices contained therein. Time **t2** denotes a valid data window reduced by the times **t1** and **t3**.

In a conventional memory system, various integrated circuit memory devices, such as memory devices **21**, **31**, and **51**, may be connected to each other and there may be differences in transmission time for signals between the memory controller **10** and the memory devices **21**, **31**, and **51** based on the position of the memory device **21**, **31**, and **51**. In addition, skew may exist between signals. The differences in signal transmission time and/or skew may increase the data setup time and/or the data

hold time, and may reduce the valid data window for determining the maximum operating frequency of the memory system.

To compensate for skew and/or the differences in signal transmission time, a memory device and/or a memory controller may use a PLL and/or a DLL. Unfortunately, incorporating a PLL and/or a DLL into memory systems may increase the size of the memory systems. Also, designing a PLL and/or DLL may increase the development complexity of memory systems.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide integrated circuit memory systems, memory controllers, memory devices, and methods of operating same. For example, in some embodiments, an integrated circuit memory system comprises one or more memory modules in which at least one of the memory modules is responsive to a control signal and has delay control information stored thereon. The memory system further comprises a memory controller that is configured to generate the control signal in response to the delay control information.

In further embodiments, the memory controller comprises a delay control register that is configured to receive and to store the delay control information therein and an output buffer that is configured to generate the control signal in response to an input control signal and the delay control information stored in the delay control register.

In still further embodiments, the memory controller comprises an input buffer that is configured to receive data from one or more of the memory modules at an input thereof and to provide the received data at an output thereof in response to the delay control information stored in the delay control register.

In other embodiments, the control signal comprises a command control signal, an address control signal, and data, and the output buffer comprises a command output buffer that is configured to generate the command control signal in response to an input command control signal and the delay control information stored in the delay control register, an address output buffer that is configured to generate the address control signal in response to an input address control signal and the delay information stored in the delay control register, and a data output buffer that is configured to generate the data in response to input data and the delay information stored in the delay control register.

In still other embodiments, at least one of the memory modules comprises a plurality of memory devices. Moreover, at least one of the memory devices comprises a delay control register that is configured to receive at least some of the delay control information and to store that information therein, an input buffer that is configured to generate a second control signal in response to the control signal output from the controller and the delay control information stored in the delay control register, and a memory cell array that is responsive to the second control signal.

Thus, in accordance with embodiments of the present invention, differences in signal transmission times between a memory controller and memory devices may be reduced by delaying signals at the memory controller and/or the memory devices. The operating frequency of a memory system may be improved by reducing signal skew between signals destined for different memory devices in the memory system.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features of the present invention will be more readily understood from the following detailed description of specific embodiments thereof when read in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic that illustrates a conventional memory system;

FIG. 2 is a timing diagram that illustrates skew between signals generated in the memory system of **FIG. 1**;

FIG. 3 is a block diagram that illustrates memory systems in accordance with embodiments of the present invention;

FIG. 4 illustrates memory controllers in accordance with embodiments of the present invention;

FIG. 5 illustrates memory devices in accordance with embodiments of the present invention; and

FIG. 6A is a timing diagram that illustrates the valid data window of a conventional memory system; and

FIG. 6B is a timing diagram that illustrates the valid data window of memory systems in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings

and will herein be described in detail. It should be understood, however, that there is no intent to limit the invention to the particular forms disclosed, but on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the claims. Like reference numbers signify like elements throughout the description of the figures. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

FIG. 3 illustrates a memory system, in accordance with embodiments of the present invention, that comprises a controller **100** and a plurality of memory modules **110**, **130**, and **150**. Memory module **110** comprises a plurality of memory devices **111**, **113**, **115**, and **117**. Memory module **130** comprises a plurality of memory devices **131**, **133**, **135**, and **137**. Memory module **150** comprises a plurality of memory devices **151**, **153**, **155**, and **157**. The memory modules **110**, **130**, and **150** further comprise serial presence detectors (SPDs), **220A**, **220B**, and **220C**, respectively.

SPD1 220A stores information on the positions of the memory devices **111**, **113**, **115**, and **117** in the memory module **110**. The **SPD1 220A** stores additional information, such as the respective wiring distances from the controller **100** to the memory devices **111**, **113**, **115**, and **117** and operating conditions that are associated with the wiring distance (*e.g.*, operation voltages based on the length and the conductivity of a wiring material). This information may be recorded in the **SPD1 220A** during design of the memory interface. **SPD2 220B** and **SPDn 220C** store similar information for memory modules **130** and **150**, respectively.

During initialization of the memory system, information on the respective memory modules **110**, **130**, and **150** is sent from the **SPD1 220A**, **SPD2 220B**, and/or **SPDn 220C** to the controller **100** through a serial bus. Therefore, the controller **100** may obtain the positions of the memory modules **110**, **130**, and **150** and the memory devices **111** through **157**.

FIG. 4 illustrates the memory controller **100** in accordance with embodiments of the present invention. The memory controller **100** comprises a delay control register **400**, an output buffer **410**, and a module selector **430**. The delay control

register **400** receives delay control information **DSP** from **SPD1 220A**, **SPD2 220B**, and/or **SPDn 220C**. The module selector **430** generates the module selection signals **MODS1** and **MODS2** for selecting a specific memory module **110**, **130**, or **150** in response to a clock signal **CLK** and a module address signal **MOD**.

The output buffer **410** comprises a delay controller **417**, a command output buffer **411**, an address output buffer **413**, and a data output buffer **415**. In other embodiments, the delay controller **417** may be viewed as a separate component from the output buffer **410**. The output buffer **410** applies a delay to an internal command signal **COMI**, an internal address signal **ADDI**, and internal write data **DATI** to generate a command signal **COM**, an address signal **ADD**, and write data **DAT**, respectively, in response to the module selection signals **MODS1** and **MODS2**. The delay that is applied by the output buffer **410** is based on the delay control information contained in the delay control register **400**.

The delay controller **417** generates an output signal specifying a delay time in response to the delay control information contained in the delay control register **400** and the module selection signal **MODS2**. The command output buffer **411** delays the internal command signal **COMI** in response to the output signal of the delay controller **417** and the module selection signal **MODS1**. The address output buffer **413** delays the internal address signal **ADDI** in response to the output signal of the delay controller **417** and the module selection signal **MODS1**. The data output buffer **415** delays the write data **DATI** in response to the output signal of the delay controller **417** and the module selection signal **MODS1**.

The memory controller **100** further comprises an input buffer **420**. The input buffer **420** comprises a delay controller **421** and a data input buffer **423**. In other embodiments, the delay controller **421** may be viewed as a separate component from the input buffer **420**. The delay controller **421** generates an output signal specifying a delay time in response to the delay control information contained in the delay control register **400** and an enable signal **EN**. The data input buffer **423** applies a delay to read data **DAT**, which are received from the memory devices **111** through **157**, in response to the output signal of the delay controller **421**. The input buffer **420** then provides the read data to other circuitry of the memory controller **100** after expiration of the delay time.

Referring again to **FIG. 3**, for purposes of illustration, it is assumed that the memory system comprises eight total memory modules, with memory modules **110**,

130, and **150** representing the first, second, and eighth modules, respectively. It will be understood, however, that memory systems may contain more or fewer memory modules in accordance with other embodiments of the present invention. During initialization of the memory system, the delay control register **400** reads the information contained in the **SPDs 220A**, **220B**, and **220C** and may associate respective transmission delay values with the memory modules **110**, **130**, through **150**, and may also associate respective transmission delay values with the memory devices **111** through **157** contained in the memory modules **110**, **130** through **150**, based on the characteristics of a signal received with respect to the memory modules **110**, **130**, through **150** and the memory devices **111** through **157** by a basic input/output system (BIOS). In other words, a transmission delay value represents a duration of time that it takes a signal to travel from the memory controller **100** to a memory module and/or a memory device.

When writing data to one of the memory modules **110**, **130**, through **150**, if the module address signal **MOD** corresponds to a memory module that has a transmission delay value associated therewith that is greater than or equal to the transmission delay values associated with the other memory modules, then the module selector **430** activates the module selection signal **MODS1** and deactivates the module selection signal **MODS2** in response to the clock signal **CLK**. Because the module selection signal **MODS2** is deactivated, the delay controller **417** is disabled. Therefore, the internal command signal **COMI**, the internal address signal **ADDI**, and the write data **DATI** may be output as the command signal **COM**, the address signal **ADD**, and data **DAT** without any delay based on the delay control information stored in the delay control register **400** being applied thereto by the output buffer **410**. In the example shown in **FIG. 3**, memory module **150** may correspond to the memory module that has the greatest transmission delay value associated therewith as it is located the farthest from the memory controller **100**. Likewise, memory device **157** may correspond to a memory device that has the greatest transmission delay value associated therewith as it is located the farthest from the memory controller **100**. It will be understood, however, that in other embodiments of the present invention, the memory module and/or the memory device with the greatest transmission delay value associated therewith may not necessarily be located the farthest distance away from the memory controller.

If, however, the module address signal **MOD** corresponds to a memory module that has a transmission delay value associated therewith that is less than one or more transmission delay values associated with other memory modules, then the module selector **430** deactivates the module selection signal **MODS1** and activates the module selection signal **MODS2** in response to the clock signal. In the example of **FIG. 3**, if the module address signal **MOD** corresponds to any memory module other than memory module **150**, then the module selection signal **MODS1** is deactivated and the module selection signal **MODS2** is activated.

The delay controller **417** generates an output signal specifying a delay time in response to the delay control information contained in the delay control register **400** and the module selection signal **MODS2**. The delay time is a value, which is determined based on previously obtained **SPD** information, for reducing skew between signals transmitted between the memory controller and the memory modules **110**, **130**, and **150**, and for reducing differences in signal delays for signals transmitted between the memory controller and the memory modules **110**, **130**, and **150**. The delay time is applied to signals received at the command output buffer **411**, the address output buffer **413**, and the data output buffer **415**. Therefore, the command signal **COM**, the address signal **ADD**, and the write data **DAT** are generated by delaying the internal command signal **COMI**, the internal address signal **ADDI**, and the write data **DATI**, respectively, by the delay time specified by the output signal of the delay controller **417**.

When reading data from one of the memory modules **110**, **130**, through **150**, if data is being read from a memory device contained in a memory module that has a transmission delay value associated therewith that is greater than or equal to the transmission delay values associated with the other memory modules (*e.g.*, memory device **157** of memory module **150** as discussed above), then the input buffer **420** may provide read data to other circuitry of the memory controller **100** without any delay based on the delay control information stored in the delay control register **400** being applied thereto by the data input buffer **423**. If, however, data is being read from a memory device contained in a memory module that has a transmission delay value that is less than one or more transmission delay values associated with other memory modules (*e.g.*, memory devices **111** through **137** of memory modules **110** and **130** as discussed above), then the delay controller **421** generates an output signal specifying a delay time in response to the delay control information contained in the delay control

register **400** and the enable signal **EN**. The data input buffer **423** applies the delay time to read data **DAT**, which are received from the memory devices **111** through **157**, in response to the output signal of the delay controller **421**. The input buffer **420** then provides the read data to other circuitry of the memory controller **100** after expiration of the delay time.

FIG. 4 illustrates methods of operating memory systems, memory controllers, and memory modules in accordance with embodiments of the present invention. Memory systems operate by controlling the delay that is applied to signals output from the memory controller **100** and destined for the memory modules **110, 130,** through **150**, and by controlling the delay that is applied to data received from the memory modules **110, 130,** through **150** at the memory controller **100**.

Delay control information **DSP** is received from the **SPD1 220A, SPD2 220B,** and/or **SPDn 220C** and is stored in the delay control register **400**. The module selector **430** activates a module selection signal **MODS1** or **MODS2** for selecting one of the memory modules **110, 130,** and **150** in response to the clock signal **CLK**. The delay controllers **417** and **421** generate respective output signals specifying a delay time in response to the delay control information contained in the delay control register **400**. The module selector **430** activates the module selection signal **MODS1** and deactivates the module selection signal **MODS2** if the memory module to be written to has a transmission delay value associated therewith that is greater than or equal to the transmission delay values associated with the other memory modules. Conversely, the module selector **430** activates the module selection signal **MODS2** and deactivates the module selection signal **MODS1** if the memory module to be written to has a transmission delay value associated therewith that is less than one or more transmission delay values associated with other memory modules. The module selection signals **MODS1** and **MODS2** control whether the output buffer **410** applies a delay time received from the delay controller **417** to the internal command signal **COMI**, the internal address signal **ADDI**, and the write data **DATI**, to generate the command signal **COM**, the address signal **ADD**, and the write data **DAT**.

If data is being read from a memory device contained in a memory module that has a transmission delay value associated therewith that is greater than or equal to the transmission delay values associated with the other memory modules (*e.g.*, memory device **157** of memory module **150** as discussed above), then the input buffer **420** may provide read data to other circuitry of the memory controller **100** without

any delay based on the delay control information stored in the delay control register **400** being applied thereto by the data input buffer **423**. If, however, data is being read from a memory device contained in a memory module that has a transmission delay value that is less than one or more transmission delay values associated with other memory modules (*e.g.*, memory devices **111** through **137** of memory modules **110** and **130** as discussed above), then the delay controller **421** generates an output signal specifying a delay time in response to the delay control information contained in the delay control register **400** and the enable signal **EN**. The data input buffer **423** applies the delay time to read data **DAT**, which are received from the memory devices **111** through **157**, in response to the output signal of the delay controller **421**. The input buffer **420** then provides the read data to other circuitry of the memory controller **100** after expiration of the delay time.

FIG. 5 illustrates the memory device **111** in more detail, in accordance with embodiments of the present invention. The other memory devices **113** through **157** may be configured similarly to memory device **111,** in accordance with embodiments of the present invention. Memory device **111** comprises a delay control register **500,** an input buffer **510**, and a memory cell array **520**. The delay control register **500** receives delay control information **DS** from the memory controller **100** and stores the received delay control information **DS**. The delay control register **500** receives the delay control information DS and sets a delay time for the memory device **111**, which is based on respective delay times for other memory devices **113** through **157**, during initialization of the memory system.

The input buffer **510** receives a command signal **COM**, an address signal **ADD**, and write data **DAT** from the memory controller **100**, which have been generated by applying a delay to the internal command signal **COMI**, the internal address signal **ADDI**, and the write data **DATI**, respectively. Note that for a memory device that has the greatest transmission delay value associated therewith (*e.g.*, memory device **157**), the command signal **COM**, the address signal **ADD**, and the write data **DAT** correspond to the internal command signal **COMI**, the internal address signal **ADDI**, and the write data **DATI**. The input buffer **510** applies a delay to the received command signal **COM**, the address signal **ADD**, and the write data **DAT**. The delay time applied by the input buffer **510** is based on the delay control information for the device **111**, which is stored in the delay control register **500**.

The input buffer **510** comprises a command input buffer **511**, an address input buffer **513**, a data input buffer **515**, and a delay controller **517**. In other embodiments, the delay controller **517** may be viewed as a separate component from the input buffer **510**. The delay controller **517** generates an output signal specifying a delay time in response to the delay control information contained in the delay control register **500** and an enable signal **EN**.

The data input buffer **515** delays the write data **DAT** by the delay time and buffers the delayed write data **DAT** in response to the output signal of the delay controller **517**. The address input buffer **513** delays the address signal **ADD** by the delay time and buffers the delayed address signal **ADD** in response to the output signal of the delay controller **517**. The command input buffer **511** delays the command signal **COM** by the delay time and buffers the delayed command signal **COM** in response to the output signal of the delay controller **517**.

In general, in a memory device that has the greatest transmission delay associated there with, the input buffer **510** does not apply any additional delay to incoming signals. For example, assuming memory device **157** has the greatest transmission delay value associated therewith, when data is written to the memory device **157**, the input buffer for memory device **157** does not apply additional delay based on delay control information stored in a delay register. By contrast, when data is written to the memory device **111**, which is close to the memory controller **100** and has a relatively short transmission delay time associated therewith, the input buffer **510** applies a relatively long delay to the received command signal **COM**, address signal **ADD**, and data **DAT**. When data is being read from one of the memory devices **111** through **157**, any additional delay time applied to the read data is controlled by the memory controller **100** as discussed hereinabove.

FIG. 5 illustrates methods of operating memory devices in accordance with embodiments of the present invention. Referring to **FIG. 5**, the delay control information **DS** is received from the memory controller **100** in the delay register **500**. The delay controller **517** generates an output signal specifying a delay time in response to the delay control information contained in the delay control register **500** and an enable signal **EN**. The input buffer **510** delays an input signal received from, for example, a memory controller by the delay time. The input signal may comprise a command signal, an address signal, and write data.

Therefore, in accordance with embodiments of the present invention, differences in signal transmission times between a memory controller and memory devices may be reduced by delaying signals at the memory controller and/or the memory devices. The operating frequency of a memory system may be improved by reducing signal skew between signals destined for different memory devices in the memory system.

FIGS. 6A and **6B** are timing diagrams that illustrate the valid data window of a conventional memory system and the valid data window of a memory system in accordance with embodiments of the present invention, respectively. **FIG. 6A** shows skew in a conventional memory system that is generated due to differences in the arrival time of signals. Accordingly, the skew may reduce the valid data window time period. Time **t1** illustrates a data setup time that is increased due to skew between signals and/or differences in signal transmission time. Time **t3** illustrates a data hold time that is increased due to skew between signals and/or differences in signal transmission time. Time **t2** denotes a valid data window reduced by the times **t1** and **t3**.

FIG. 6B shows the valid data window according to embodiments of the present invention. Time **t1'** illustrates a data setup time that is increased due to skew between signals and/or differences in signal transmission time. Time **t3'** illustrates a data hold time that is increased due to skew between signals and/or differences in signal transmission time. Time **t2'** denotes a valid data window reduced by the times **t1'** and **t3'**.

Because times **t1'** and **t3'** are less than times **t1** and **t3** of **FIG. 6A**, respectively, the valid data window time period may be shorter than that provided by conventional memory systems. Accordingly, memory systems, in accordance with embodiments of the present invention, may operate at higher frequencies.

Many variations and modifications can be made to the preferred embodiments without substantially departing from the principles of the present invention. All such variations and modifications are intended to be included herein within the scope of the present invention, as set forth in the following claims.